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Docket No.: L&L-I0178


MICHAEL BURNS

Date: November 28, 2001

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Enclosed herewith are the necessary papers for filing the following application for Letters
Patent:

Applicant : LOTHAR RISCH ET AL.

Title : DOUBLE GATE MOSFET TRANSISTOR AND METHOD FOR THE
PRODUCTION THEREOF

3 sheets of formal drawings.

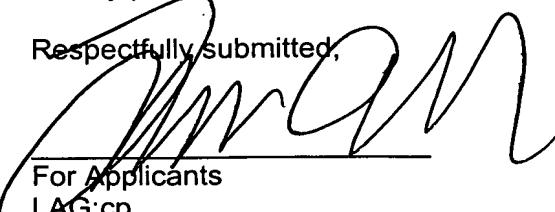
The payment in the amount of \$830.00 covering the filing fee.

PCT Cover Sheet WO 00/74143 A1.

This application is being filed without a signed oath or declaration under the provisions of 37
CFR 1.53(f). Applicants await notification of the date by which the oath or declaration and
the surcharge are due, pursuant to this rule.

The Patent and Trademark Office is hereby given authority to charge Deposit Account No.
12-1099 of Lerner and Greenberg, P.A. for any fees due or deficiencies of payments made
for any purpose during the pendency of the above-identified application.

Respectfully submitted,


For Applicants
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(12) NACH DEM VERTRAG ÜBER DIE INTERNATIONALE ZUSAMMENARBEIT AUF DEM GEBIET DES PATENTWESENS (PCT) VERÖFFENTLICHTE INTERNATIONALE ANMELDUNG

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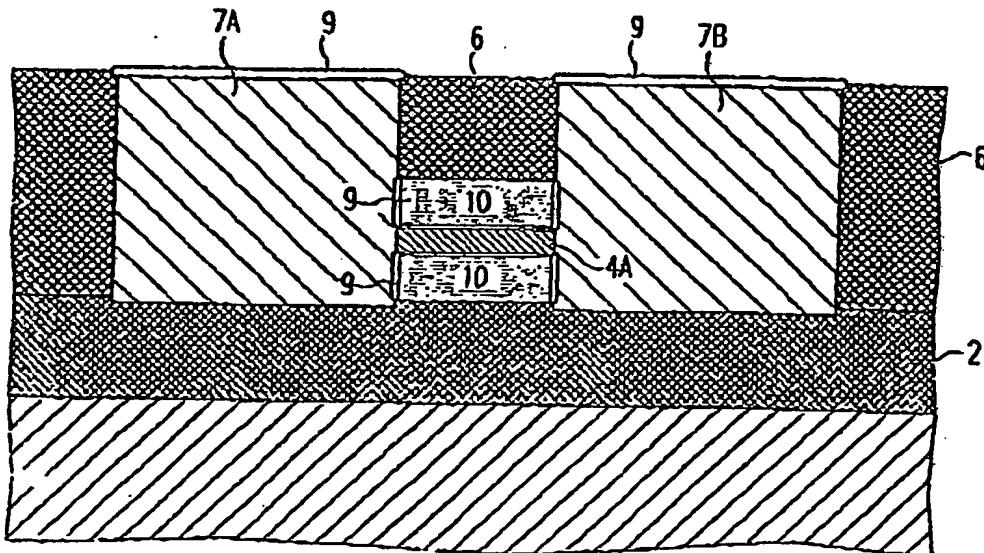
(71) Anmelder (für alle Bestimmungsstaaten mit Ausnahme von US): INFINEON TECHNOLOGIES AG [DE/DE]; St. Martin-Str. 53, D-8154 München (DE). Veröffentlichung: Mit internationalem Recherchenbericht.

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[Fortsetzung auf der nächsten Seite]

(54) Titel: DOUBLE GATE MOSFET TRANSISTOR AND METHOD FOR THE PRODUCTION THEREOF

(54) Bezeichnung: DOPPEL-GATE-MOSFET-TRANSISTOR UND VERFAHREN ZU SEINER HERSTELLUNG



(57) Abstract: The invention relates to a double gate MOSFET transistor and to a method for the production thereof. According to the invention, a semiconductor layered structure (4A) of a transistor channel to be formed is embedded in a placeholder material (3, 5) and is contacted by source (7A) and drain regions (7B) which are placed in recesses that are etched on opposing sides of the semiconductor layered structure (4A). In addition, the placeholder material (3, 5) is selectively etched out and is replaced by the electrically conductive gate electrode material (10).

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